30nm and 20nm Physical Gate Length CMOS Transistors

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Components Research

Logic Technology Development

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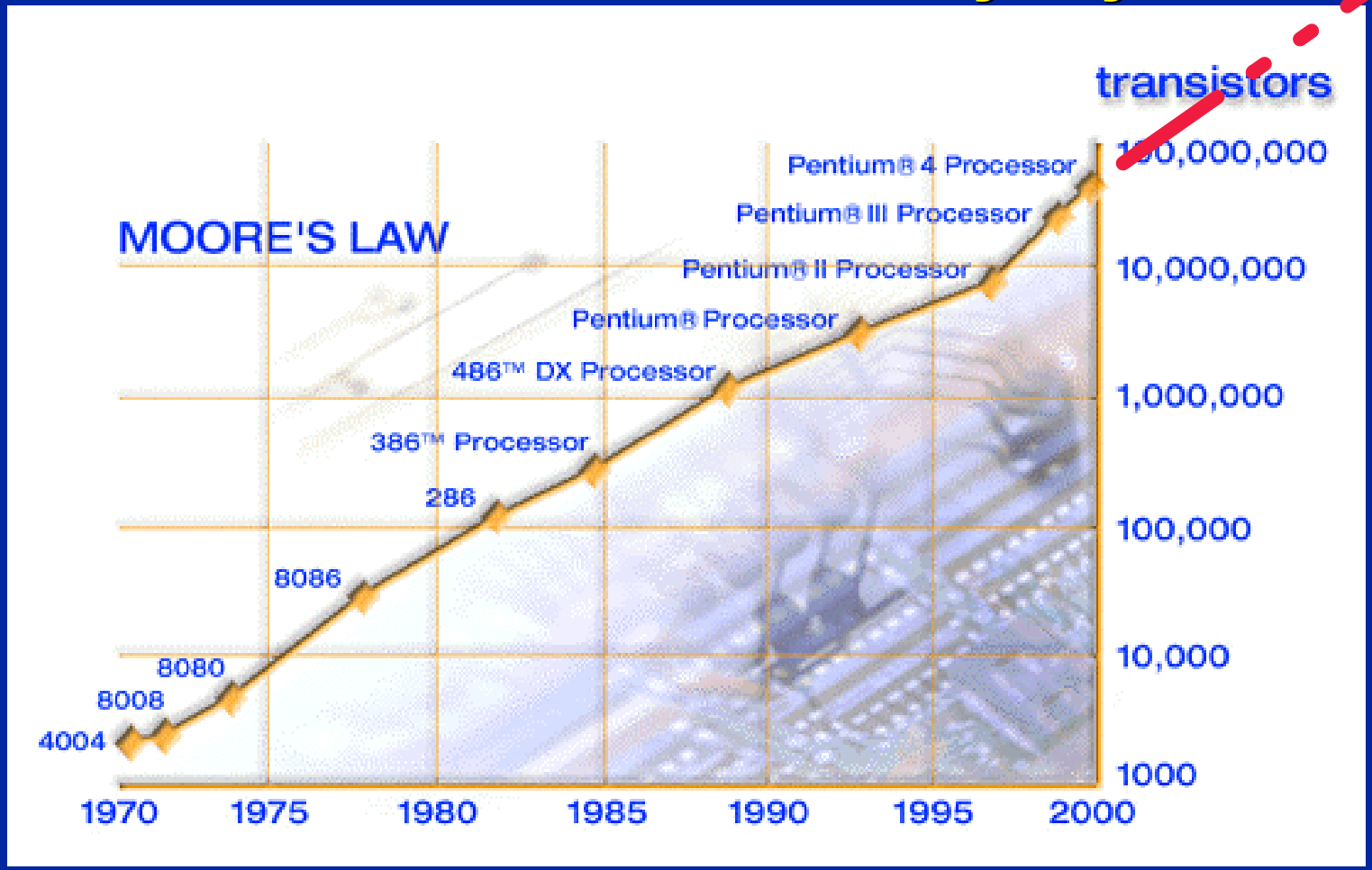
June 10, 2001

Content

- Overview
- Review on 30nm CMOS transistors
- Supply voltage scaling
- 20nm transistor research
- Summary

Moore's Law Continues

Transistors doubles every 2 years

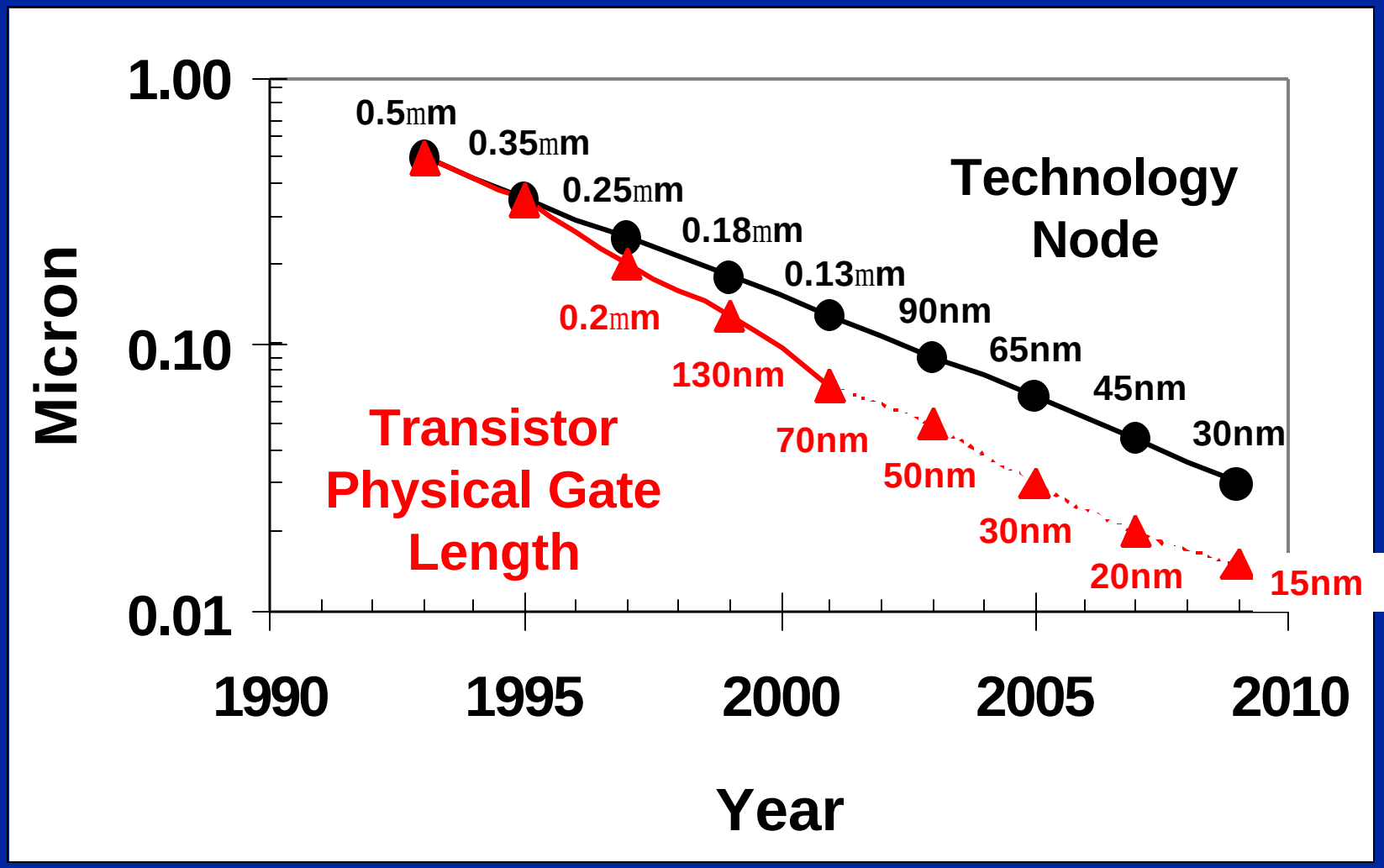


- ~1.0 billion transistors by 2007

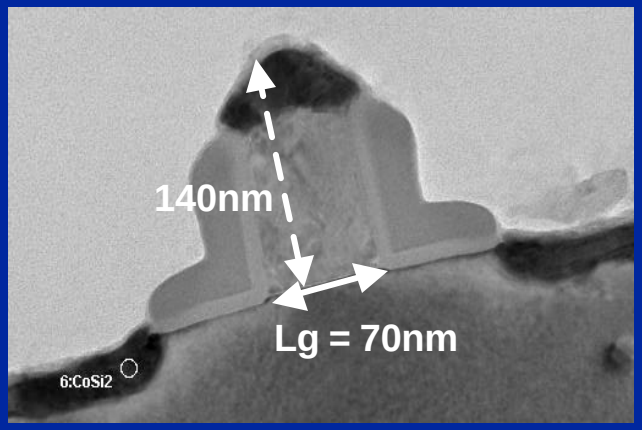
Moore's Law Drives Transistor R&D

- Transistor and supply voltage scaling are key
- 30% shrink in transistor size every 2 years
  - 2X die per wafer
  - 1/2X transistor cost
  - >30% transistor performance improvement
- >15% reduction in supply voltage every generation
  - Low operating voltage allows low power and long battery life

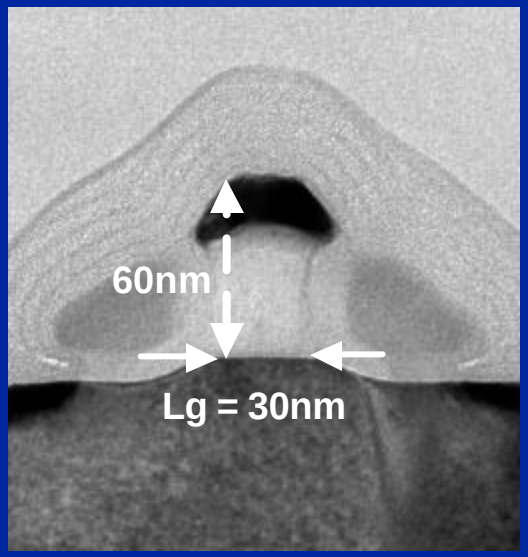
Transistor Physical Gate Length Trend (Lithography generation > L_{GATE})



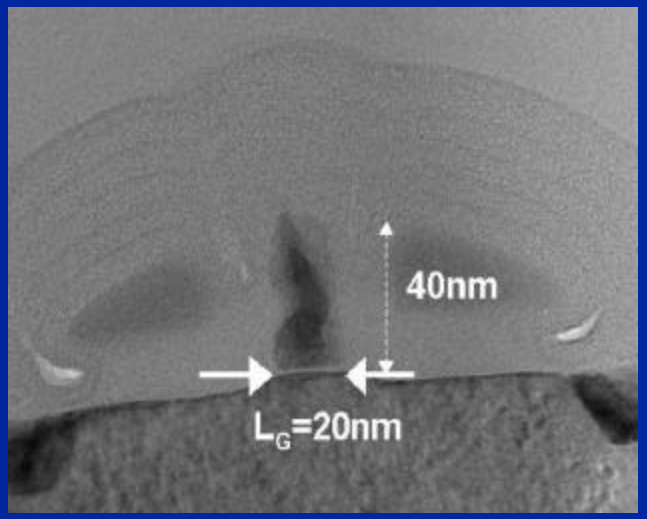
Transistor Scaling Continues



70nm transistor
(in production)

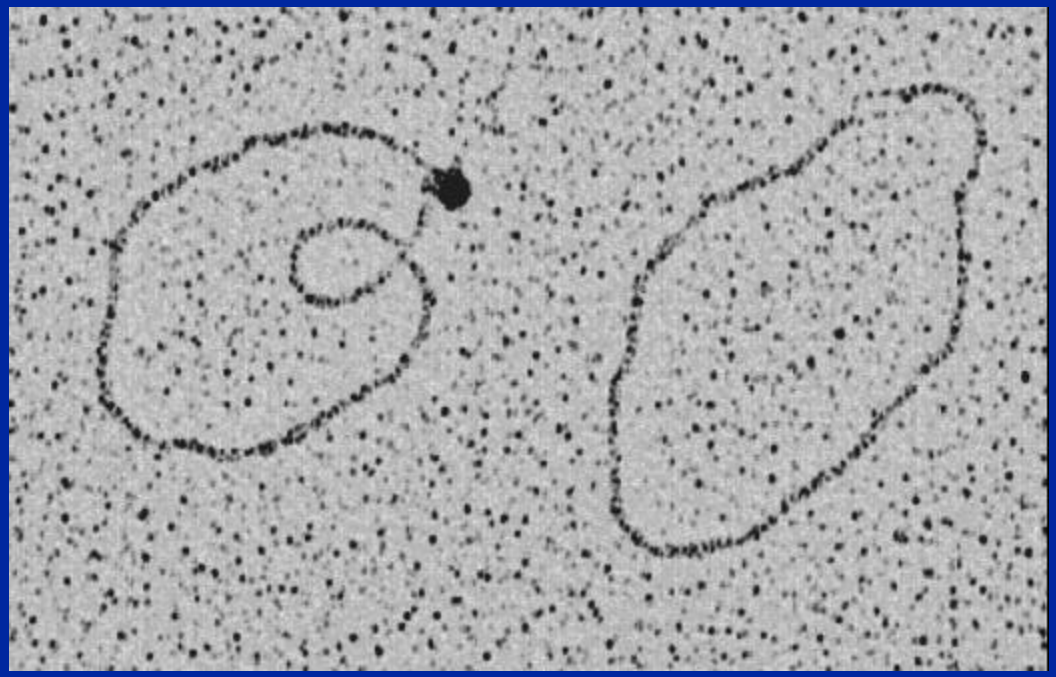


30nm transistor
(production 2005)

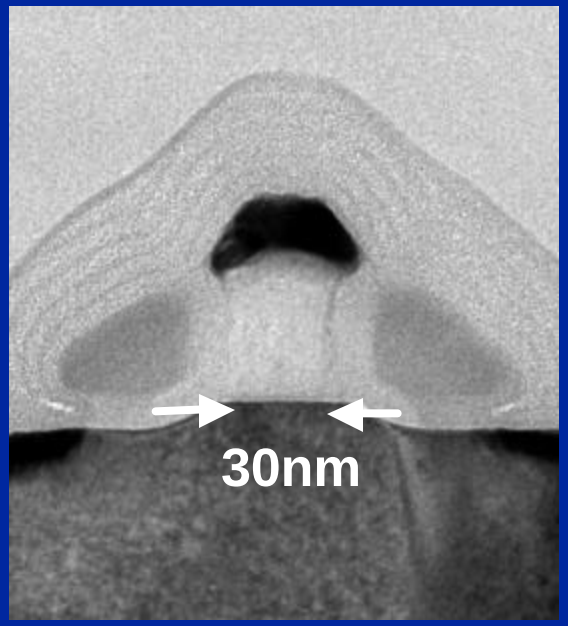


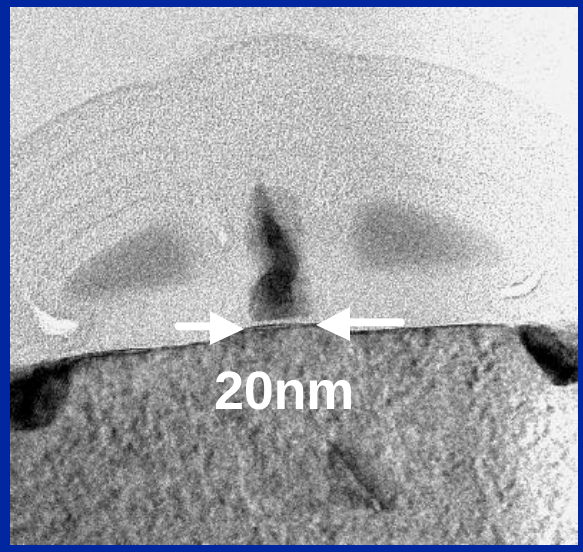
20nm transistor
(research phase)

Transistors as Small as DNA



10nm Gold particle attached to Z-DNA Antibody [John Jackson & Inman. Gene 1989 84 221-226]





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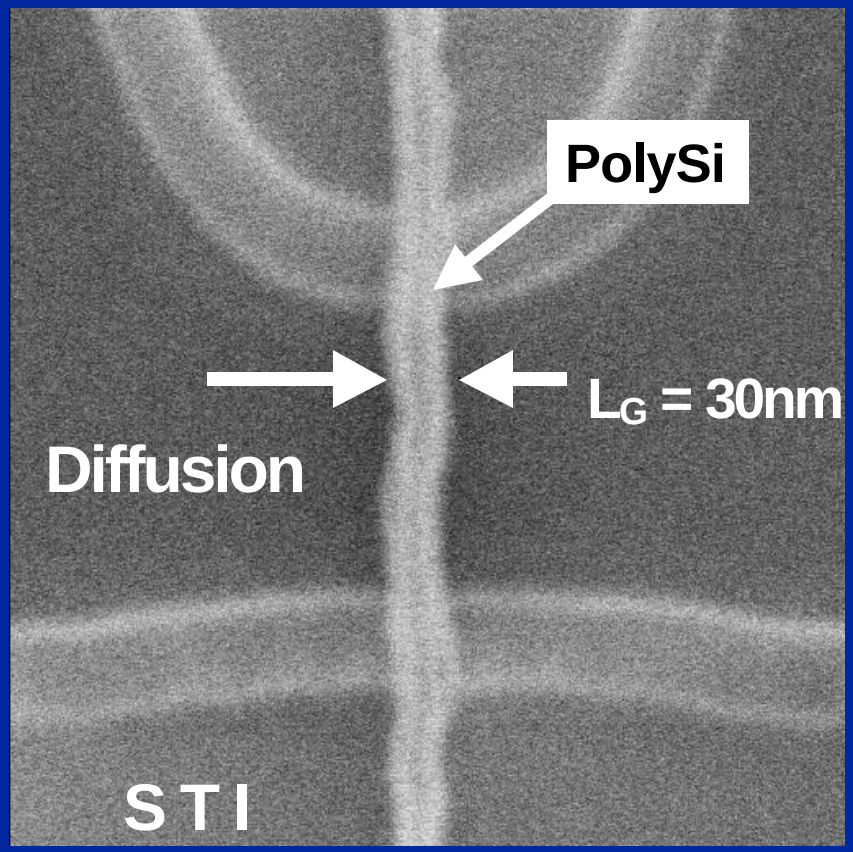
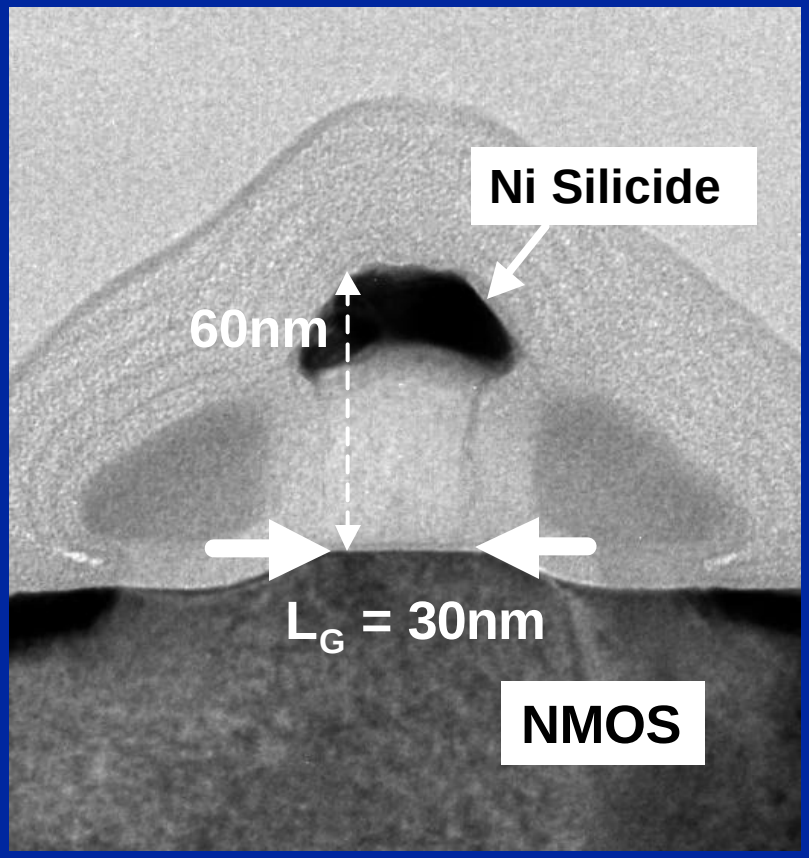
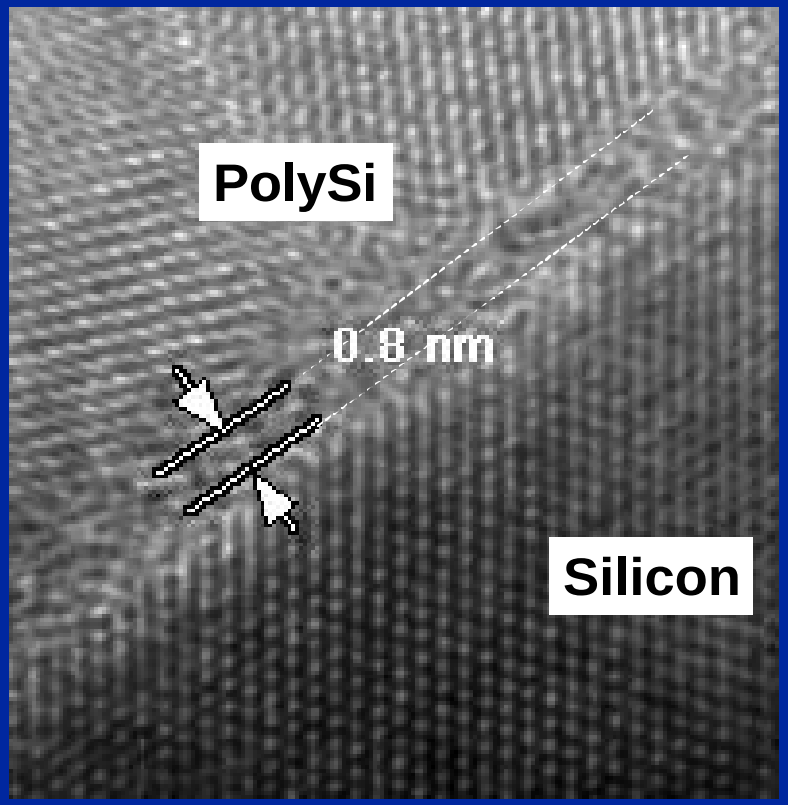
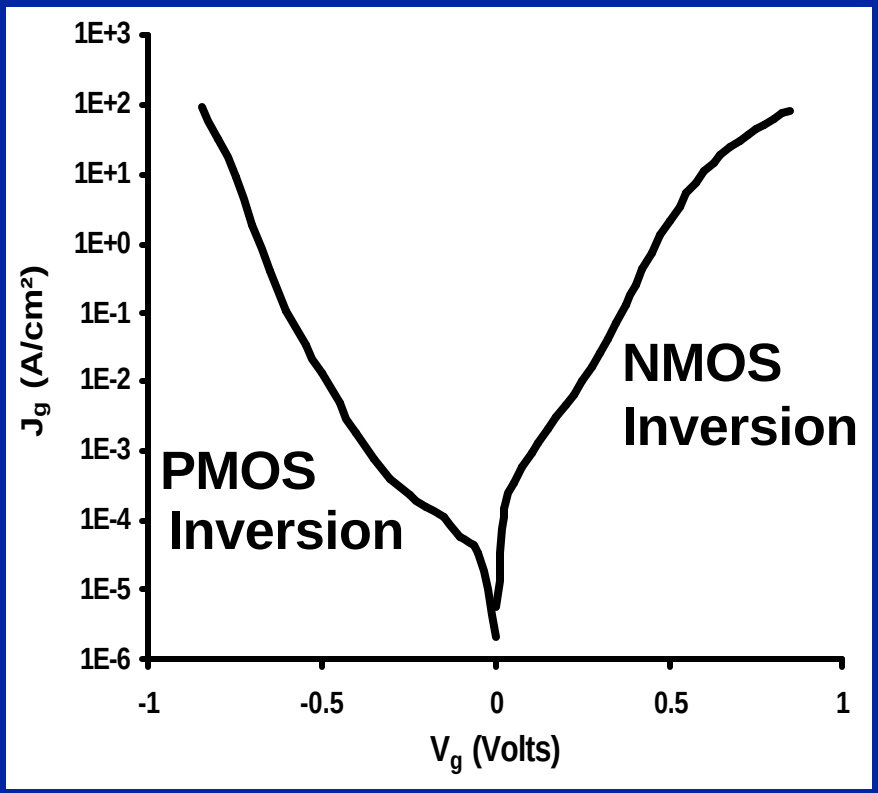
30nm Physical Gate Length Transistor





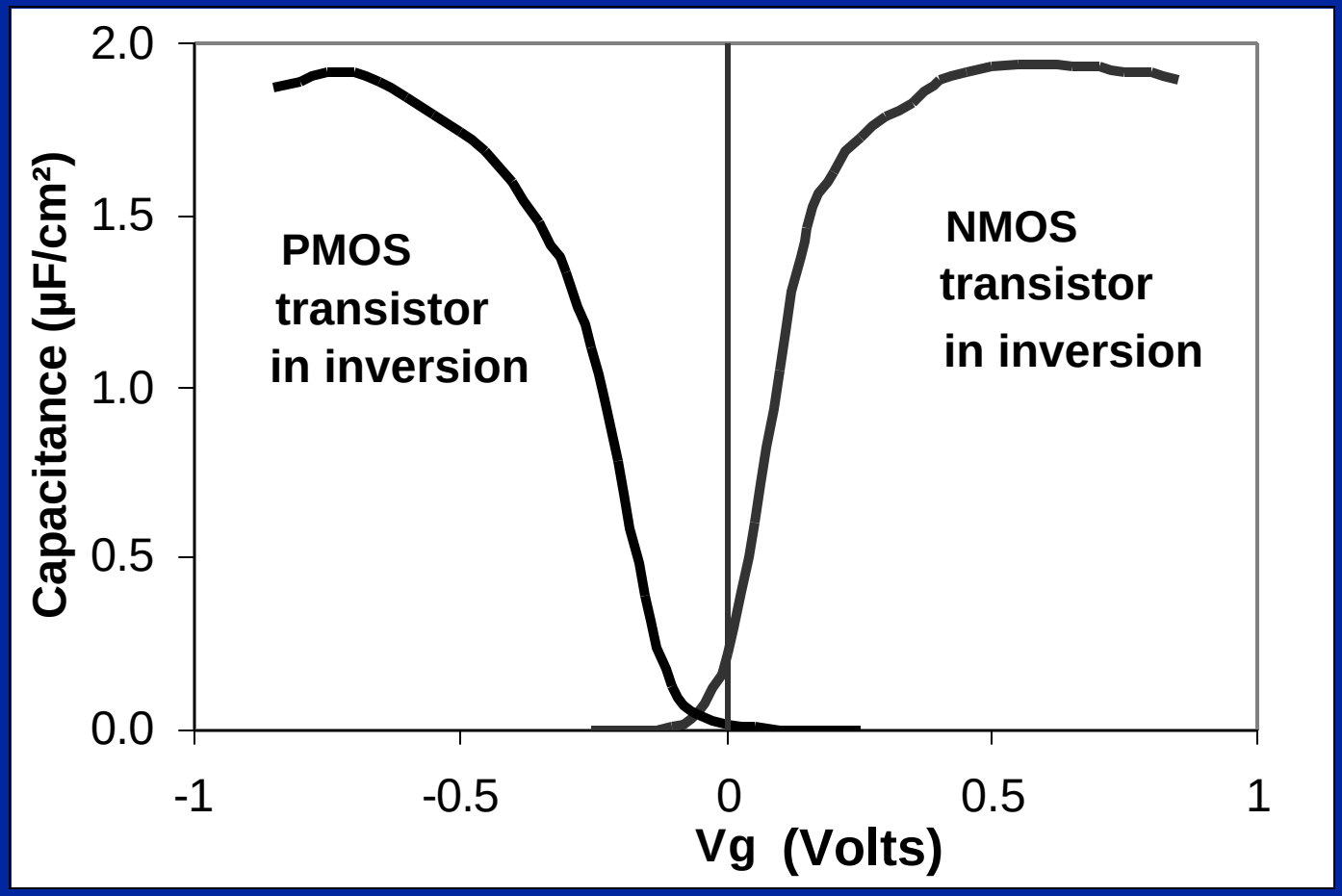
0.8nm Gate Oxide



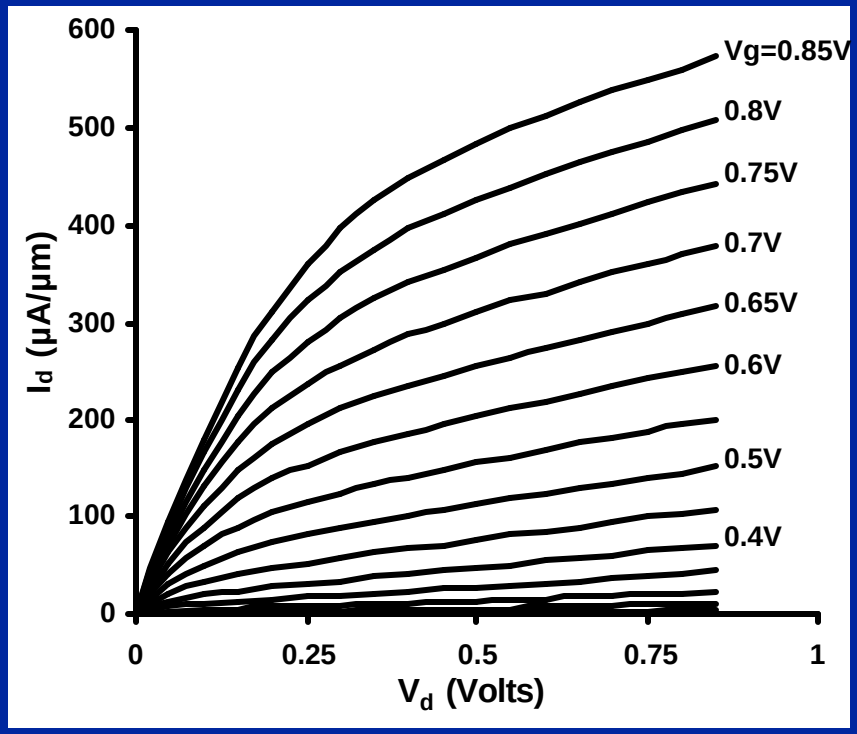


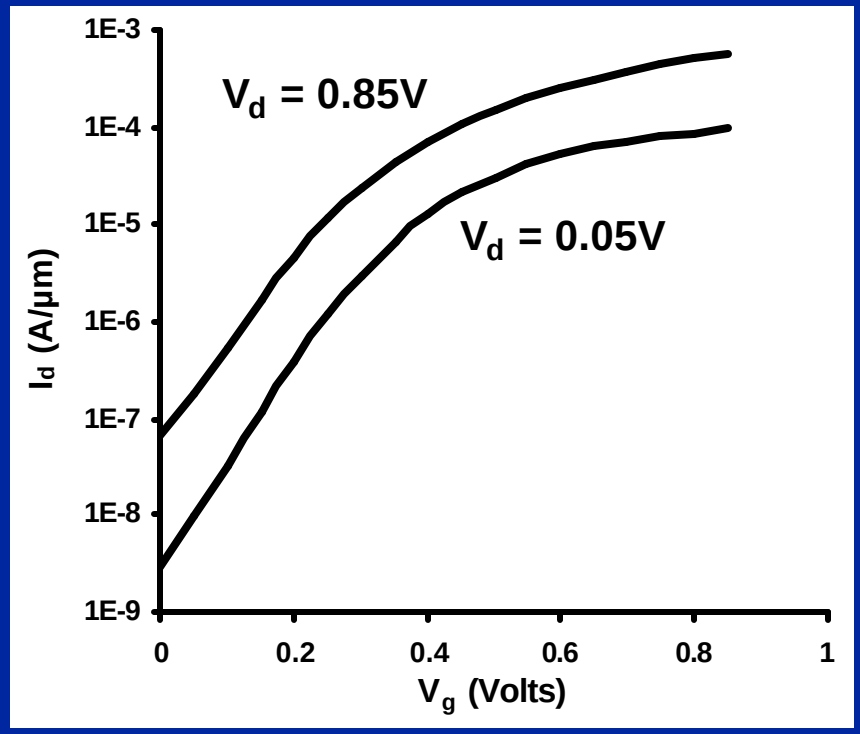
- 0.8nm gate oxide
- Gate oxide leakage ~25nA/um for 30nm L_G NMOS and PMOS at 0.85V inversion (room temperature)

Transistor Gate Inversion Capacitance for 0.8nm Gate Oxide



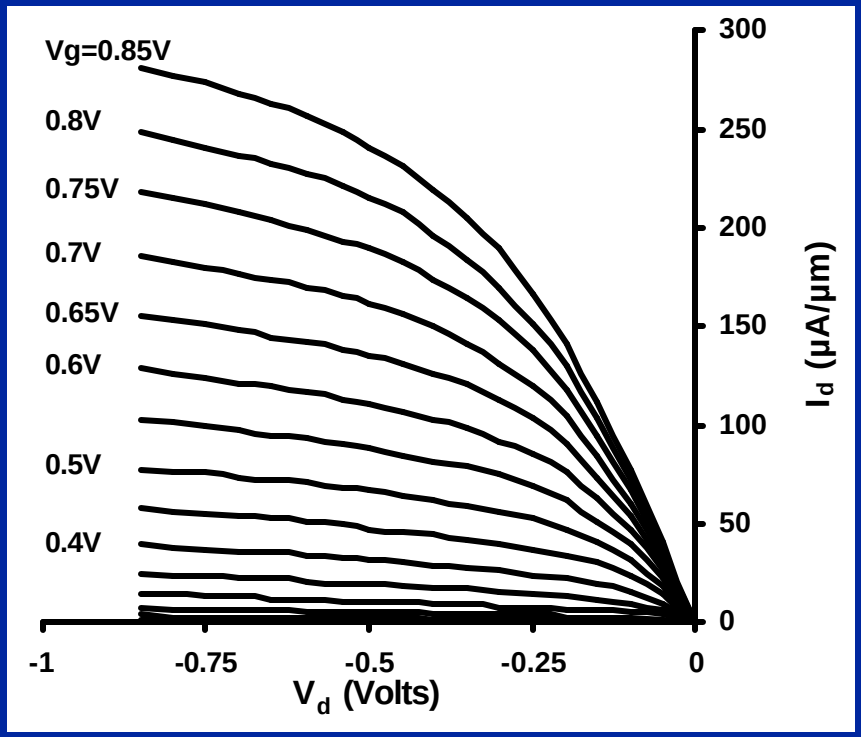
30nm L_G NMOS Transistor

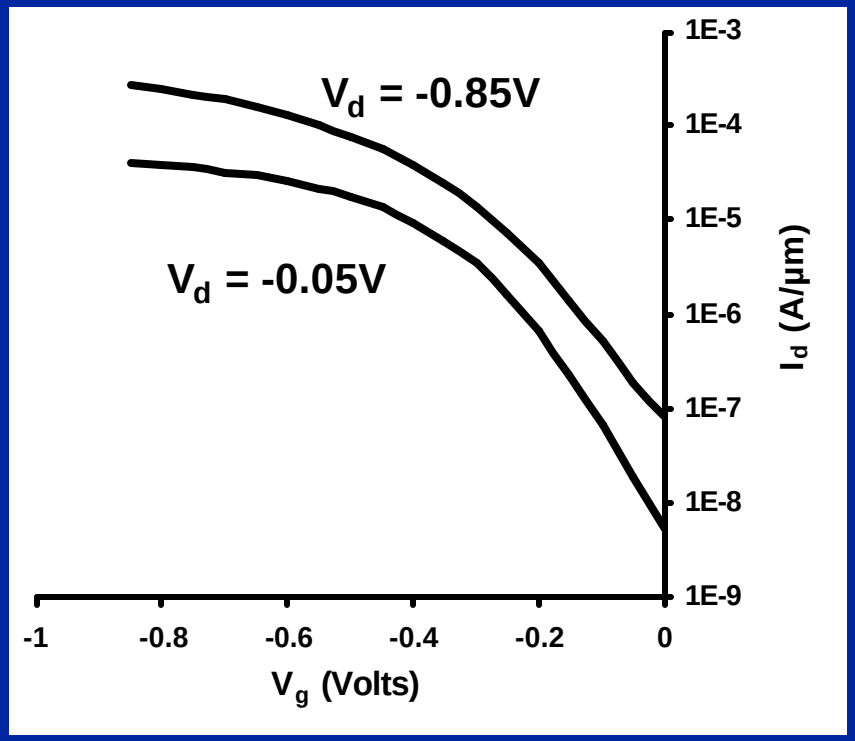




- I_{on} = 0.57mA/μm, I_{off} = 60nA/μm at V_{DD} = 0.85V
- Subthreshold slope = 100mV/decade
- DIBL = 125mV/V

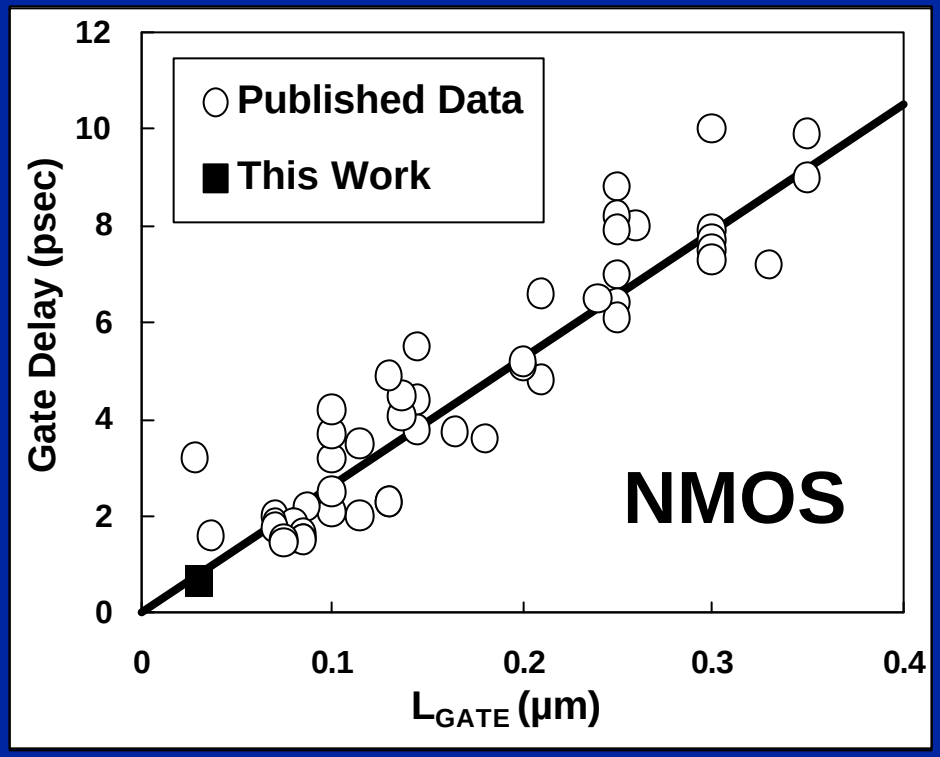
30nm L_G PMOS Transistor

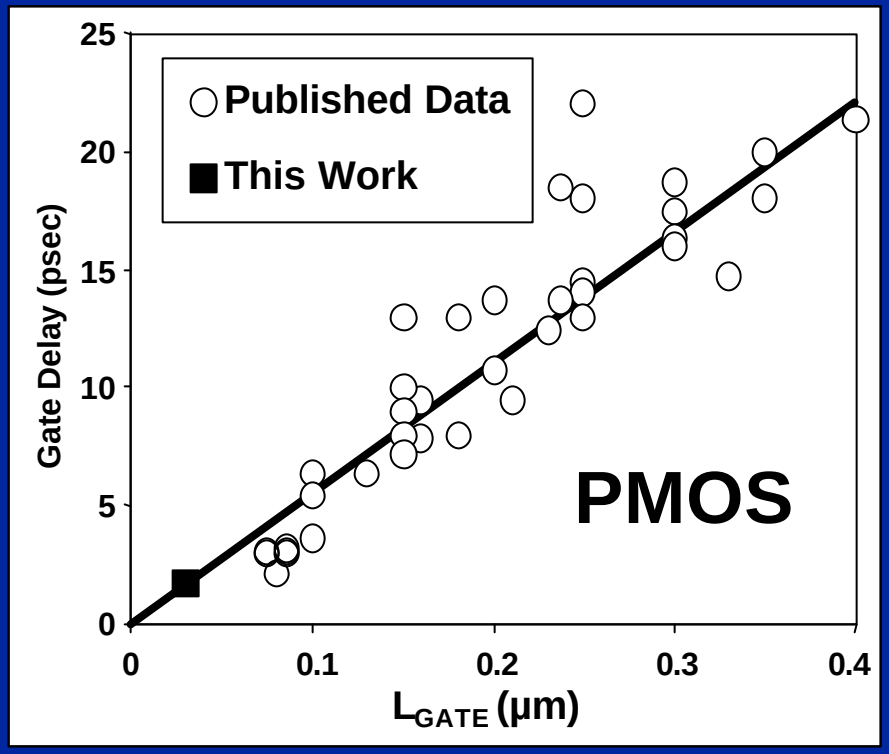




- I_{on} = 0.28mA/㎜, I_{off} = 80nA/㎜ at V_{DD} = 0.85V
- Subthreshold slope = 100mV/decade
- DIBL = 125mV/V

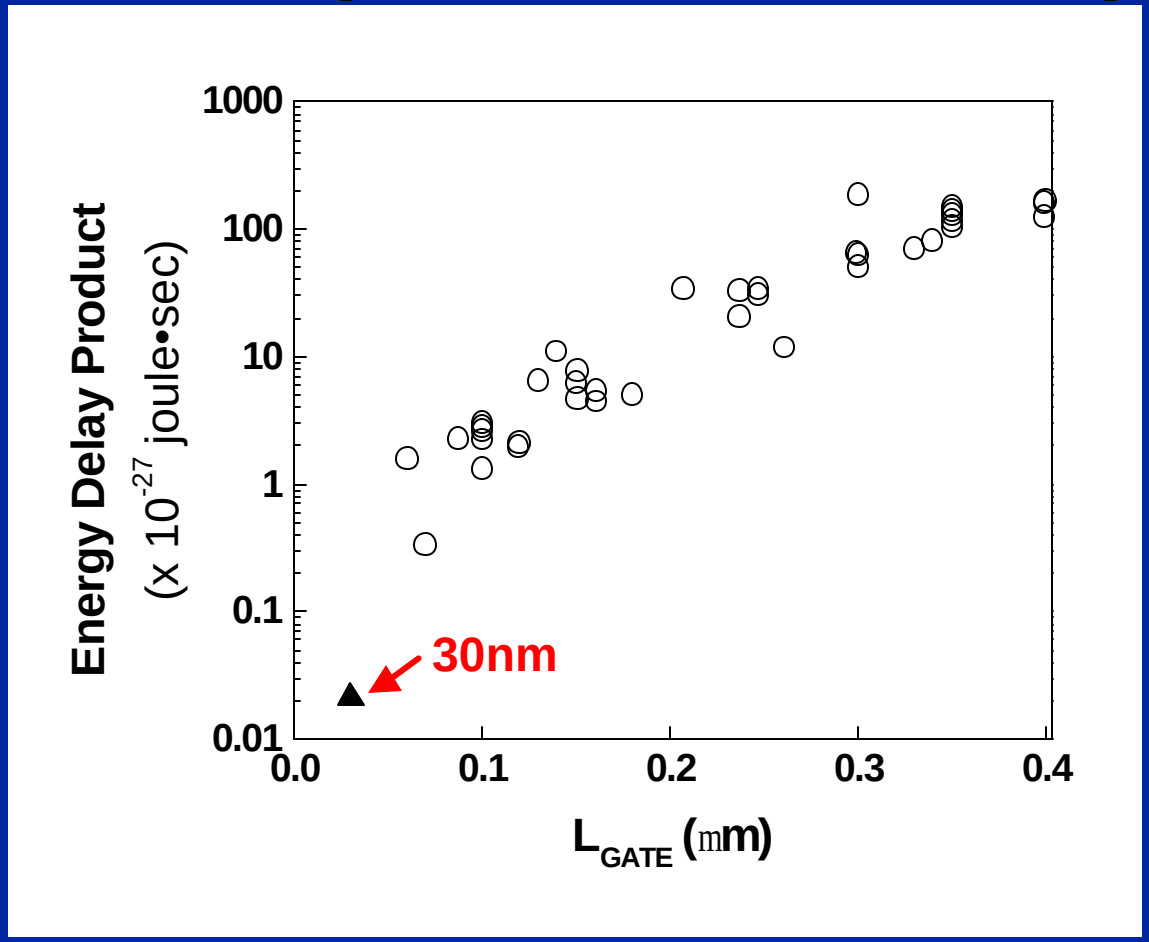
30nm Transistor CV/I Gate Delays





- NMOS gate delay = 0.85ps, PMOS gate delay = 1.7ps
- Gate delays continue to follow historical trends

NMOS Energy Delay Product
(*CV2 X CV/I*) ------ Power and Speed



- Energy delay product reduces due to supply voltage and physical gate length scaling

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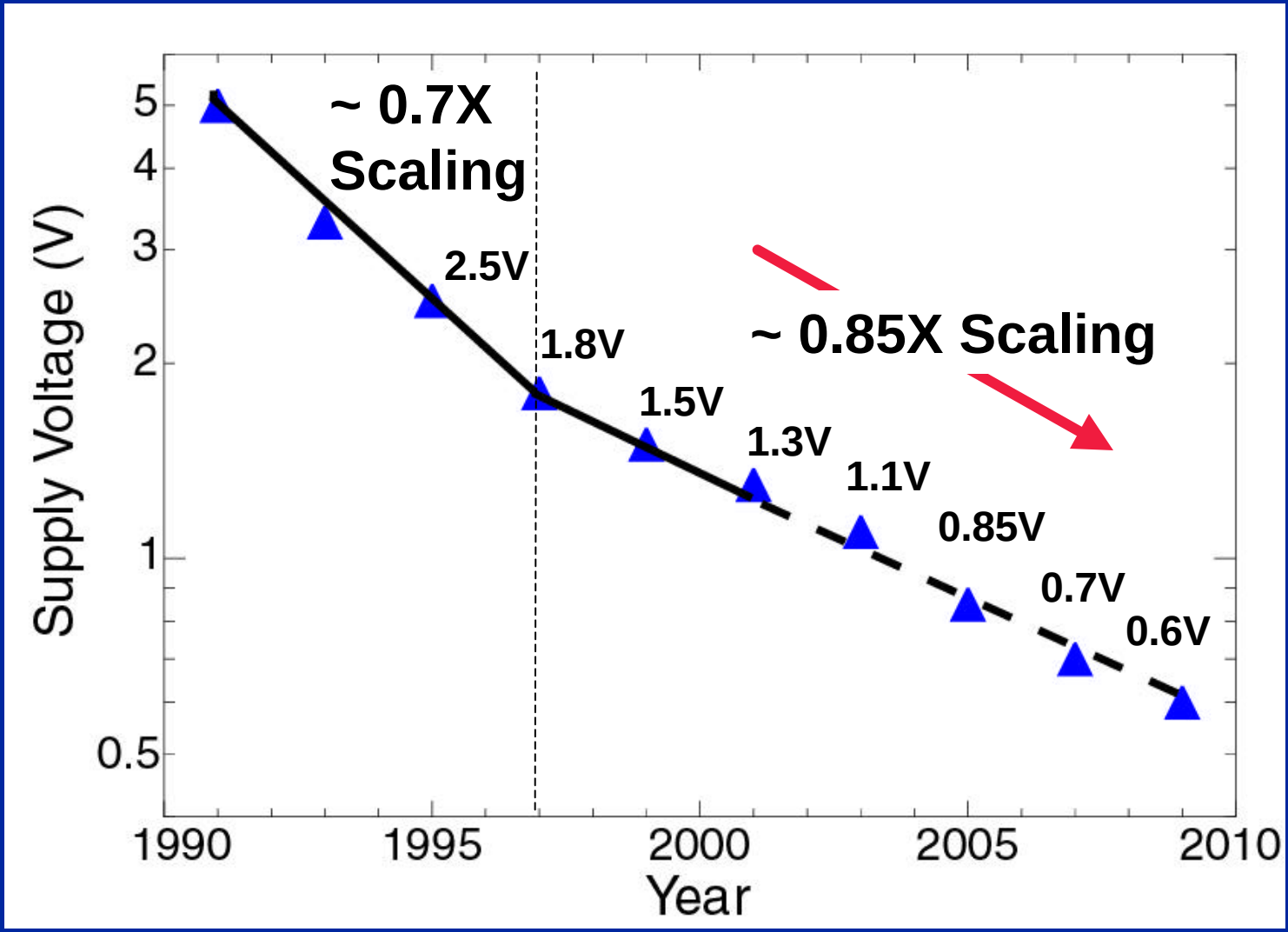
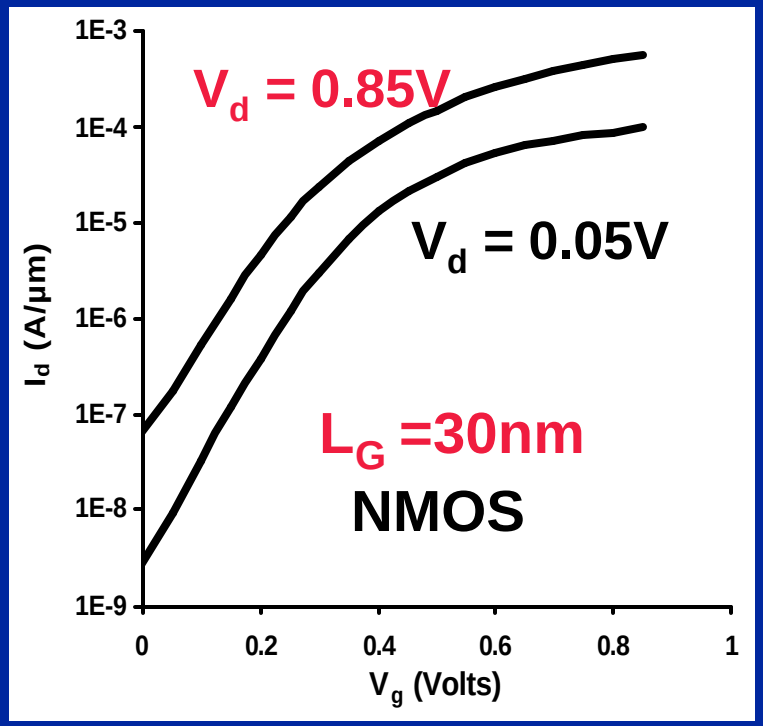
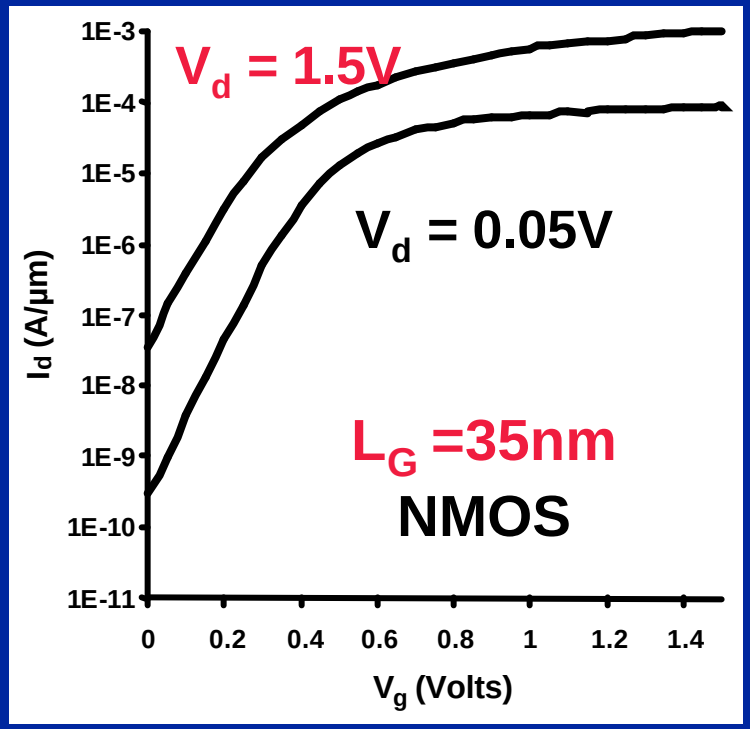
Supply Voltage Scaling Trend



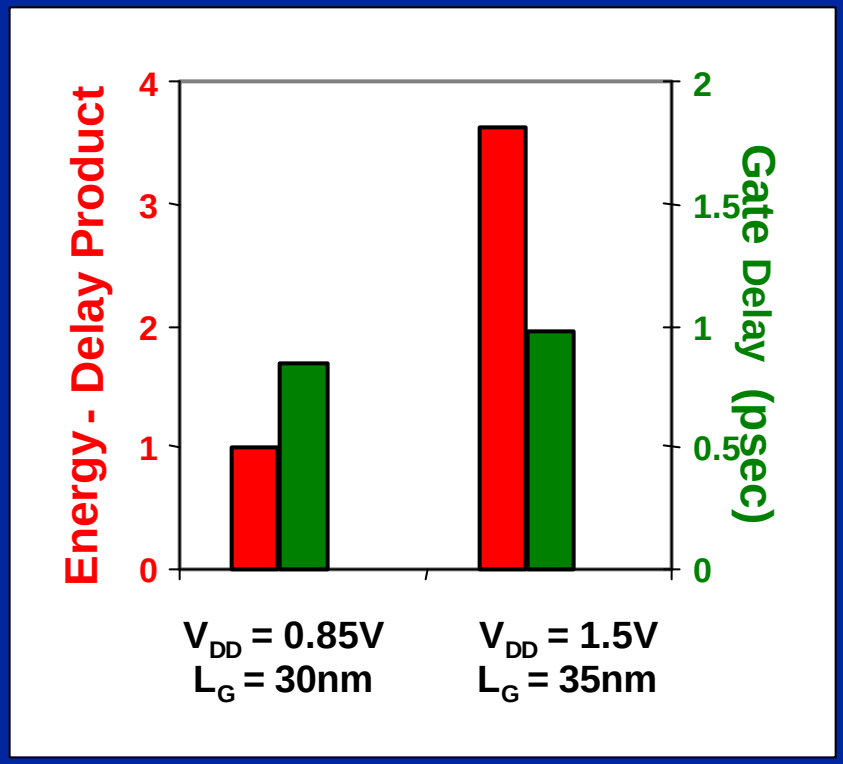
30nm L_G @ 0.85V Versus 35nm L_G @ 1.5V





- 35nm NMOS at V_{DD} = 1.5V
  - I_{on} = 1.1mA/μm, I_{off} = 50nA/μm, gate delay = 0.90ps
- 30nm NMOS at V_{DD} = 0.85V
  - I_{on} = 0.57mA/μm, I_{off} = 60nA/μm, gate delay = 0.85ps

Importance of Low V_{DD}: Energy-Delay Product



Energy-Delay Product:

$CV^2 \times CV/I = C^2V^3/I$

- **35nm NMOS @ 1.5V has >3.5X higher energy-delay product than 30nm NMOS @ 0.85V**
- **The choice of low V_{DD} (<1.0V) is important for the 65nm technology node and beyond**

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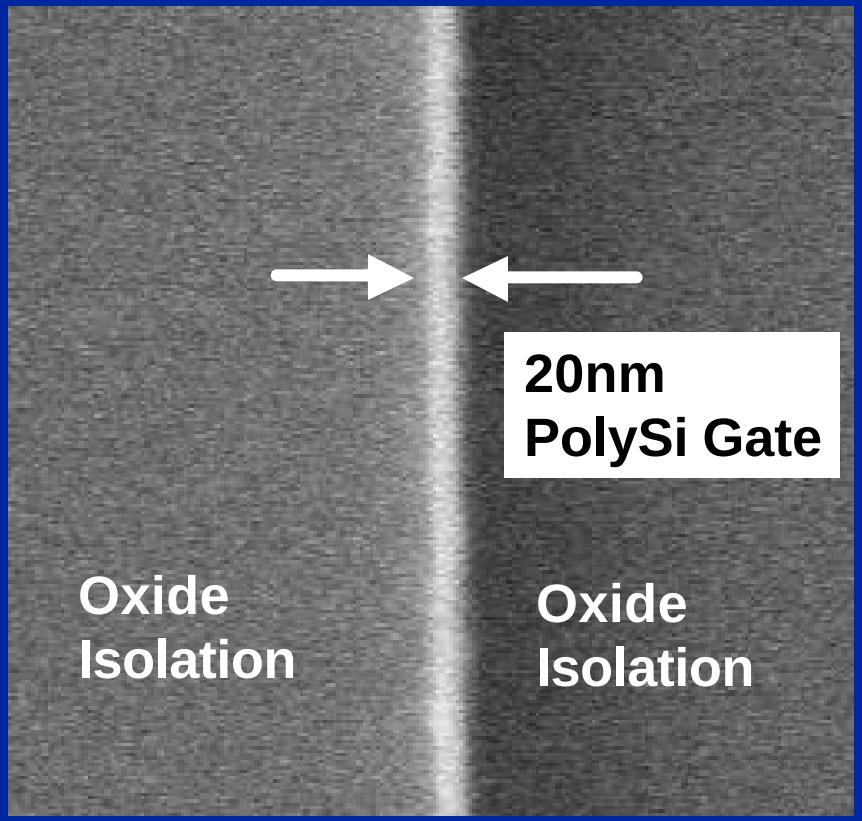
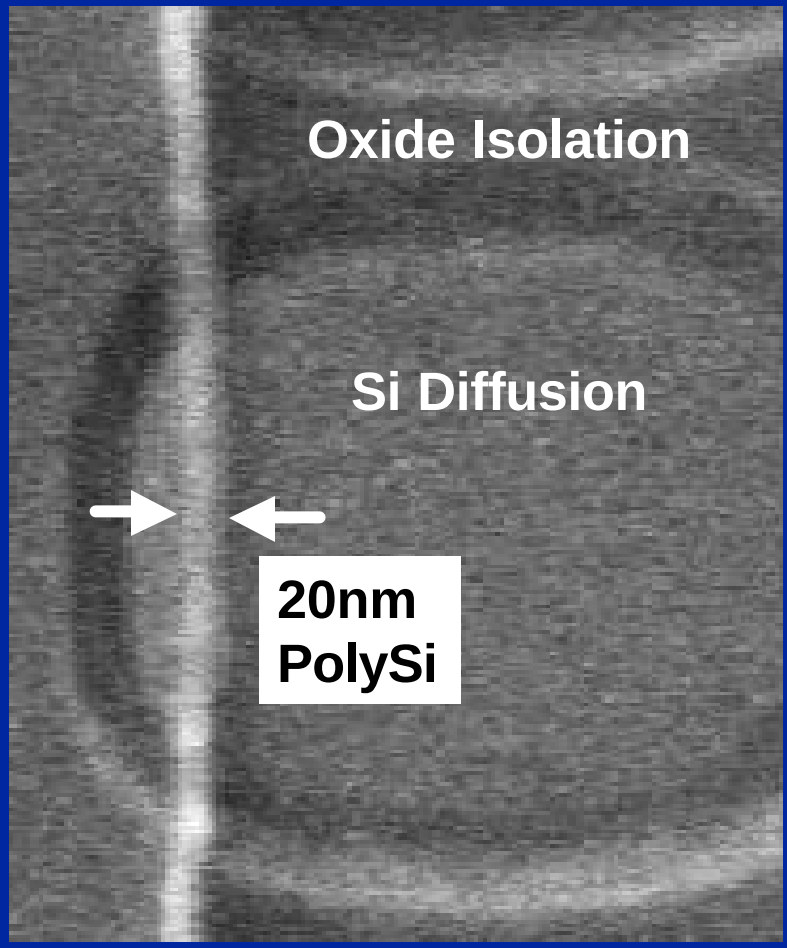
20nm Transistor Research

- **45nm technology node in production 2007**
  - **Transistor physical gate length ~20nm**
  - **Transistor research for 45nm logic technology node in progress**
- **20nm planar CMOS transistors one of the many research topics**
  - **20nm planar CMOS transistors fundamentally feasible? (YES)**
  - **Gate oxide thickness approaching zero for Tox scaling beyond 0.8nm**
    - **Alternative gate stack**

20nm Physical PolySi Gate

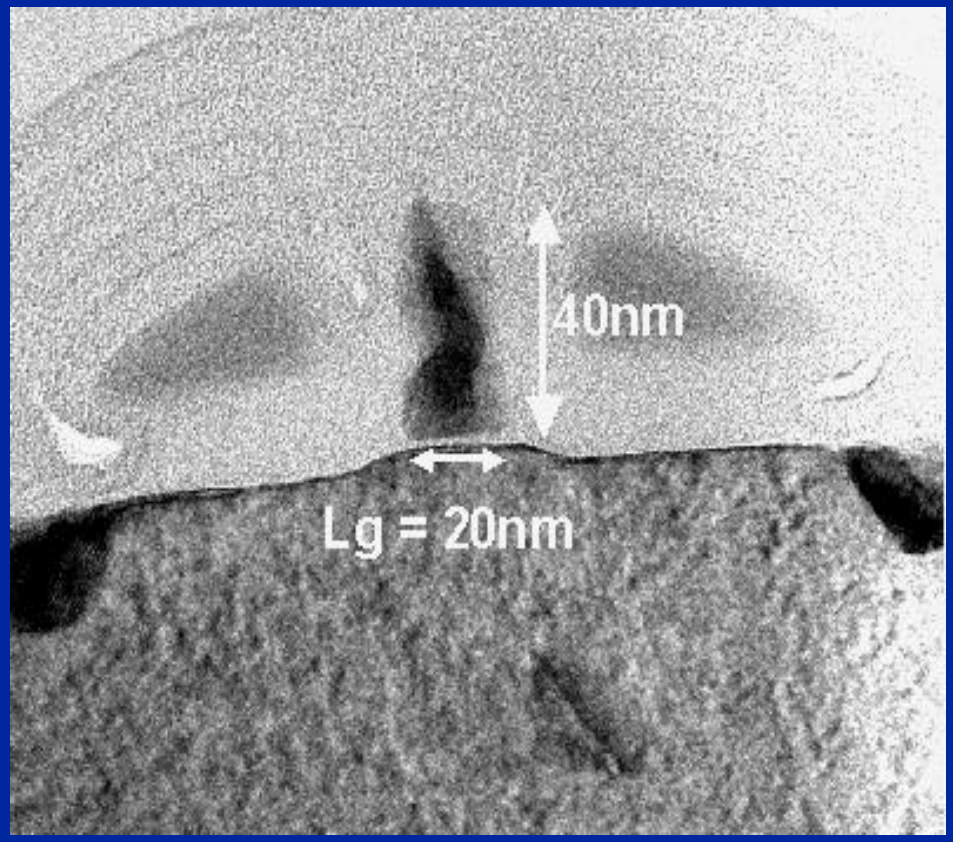


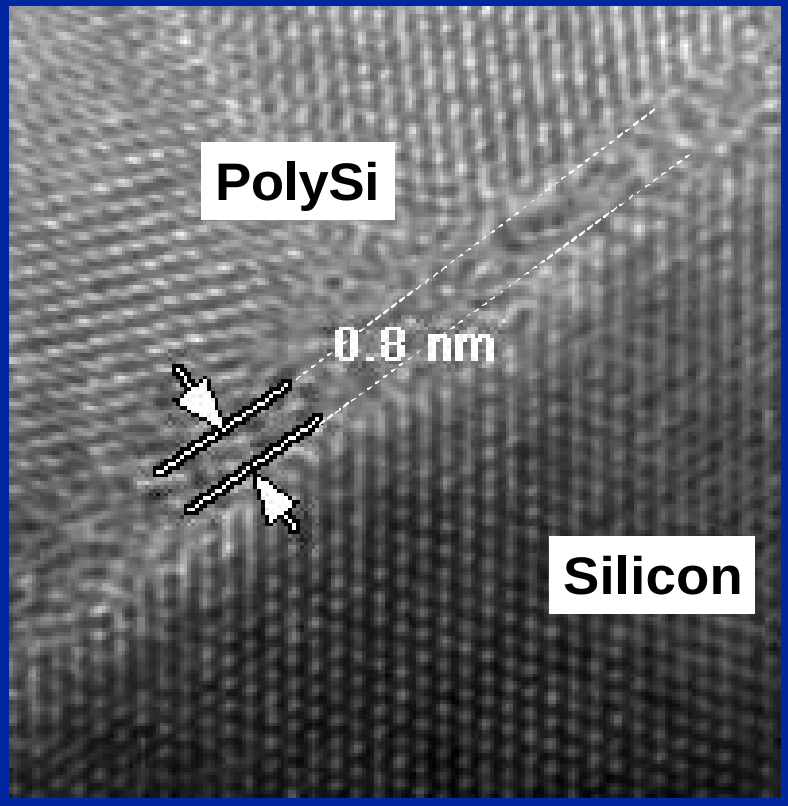
20nm polySi gate on oxide isolation



20nm polySi gate on oxide isolation and Si diffusion

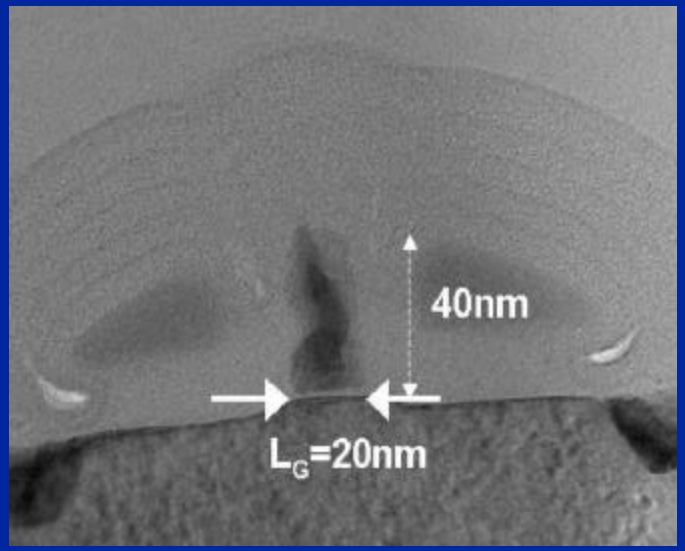
20nm Physical Gate Length NMOS Transistor

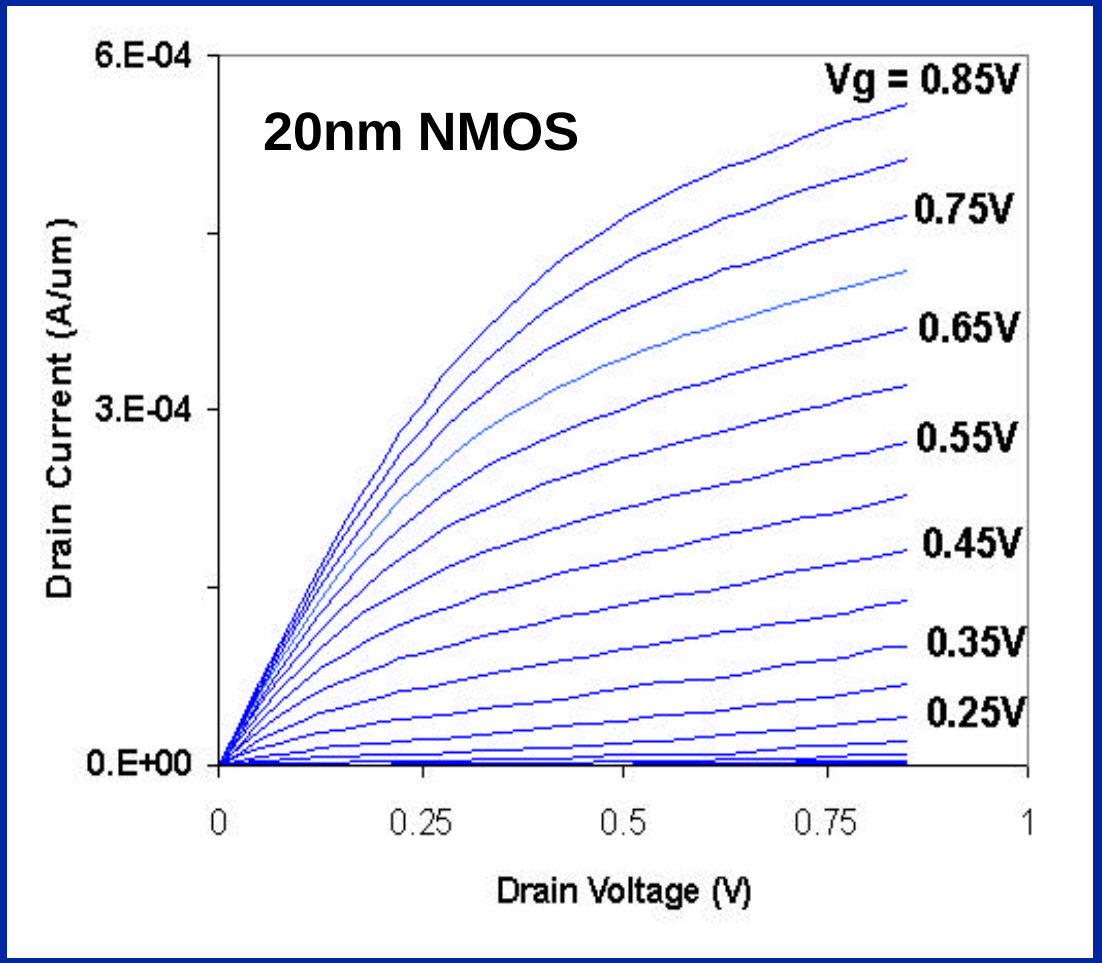




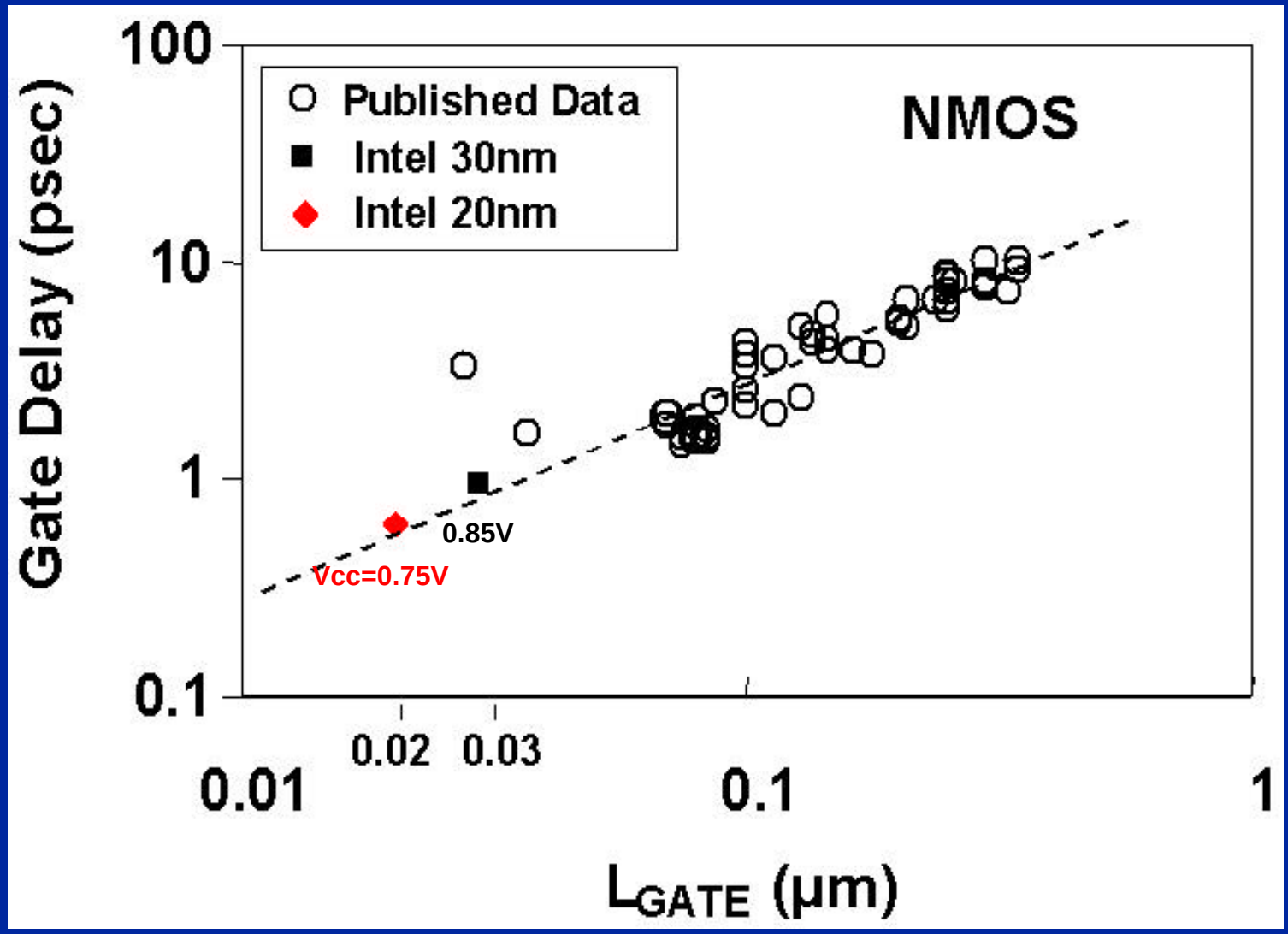
- 0.8nm conventional gate oxide

20nm Physical Gate Length NMOS Transistor

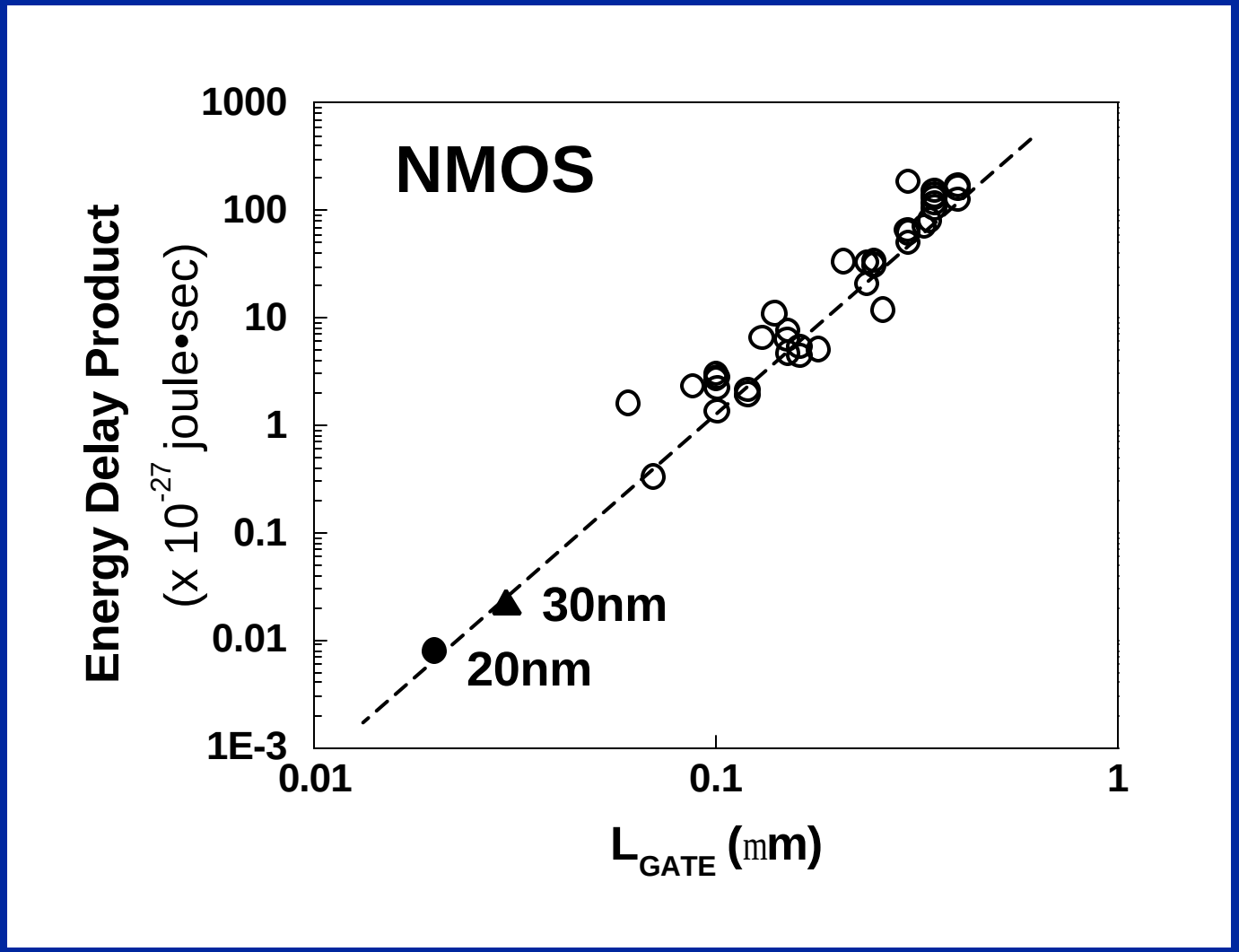




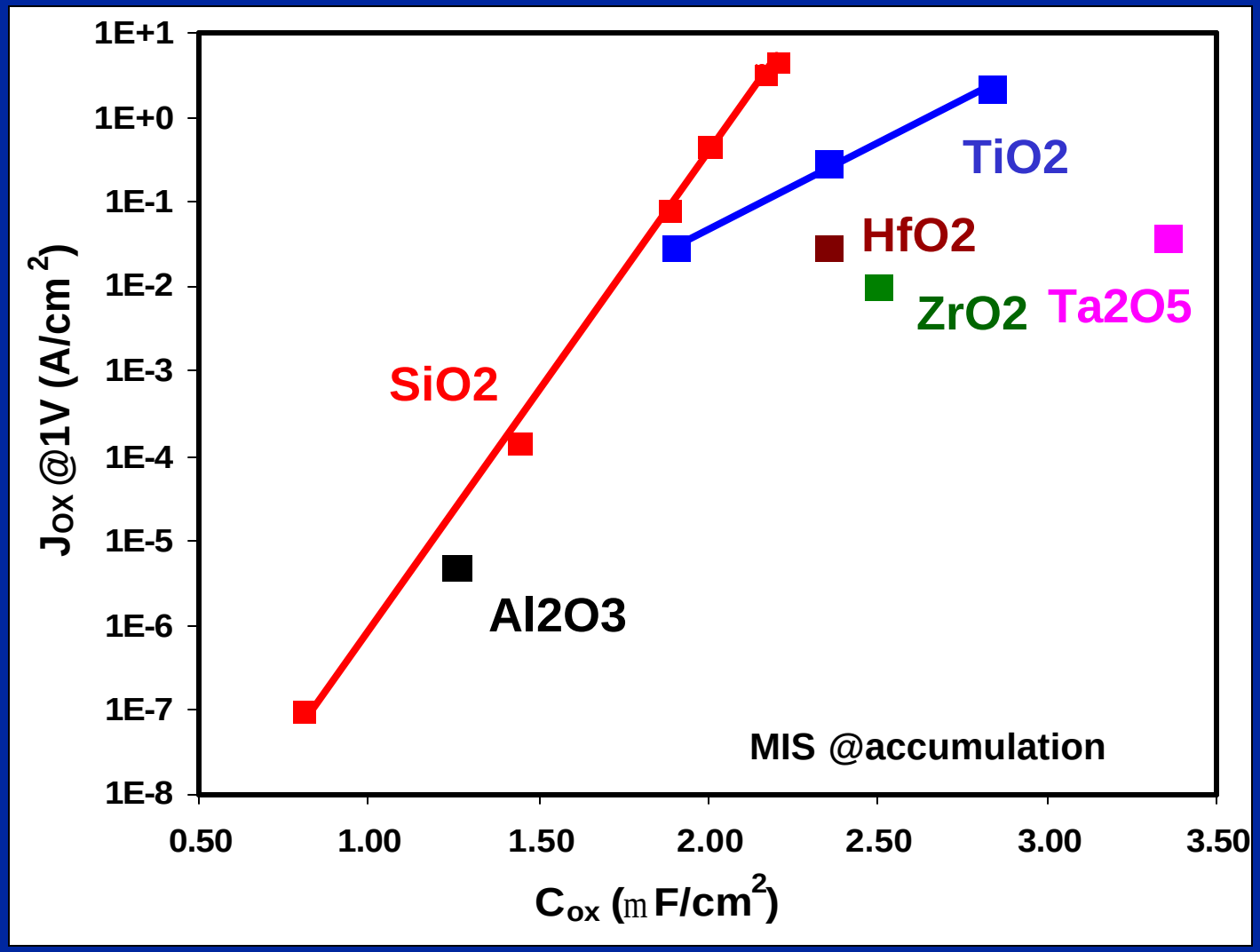
Gate Delay Trend Continues



Energy Delay Product Trend Continues



Alternative Gate Dielectrics



Summary

- High-performance 30nm physical gate length CMOS transistors have been demonstrated for the 65nm technology node, which will be ready for production 2005
- Research on 20nm physical gate length transistor and related topics are being conducted for the 45nm technology node